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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/603,382	06/24/2003	Massimo Civilini	CSCO-7199	2846

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EXAMINER	
SUGLO, JANET L	

ART UNIT	PAPER NUMBER
2857	

DATE MAILED: 05/01/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

HA

Office Action Summary	Application No.	Applicant(s)	
	10/603,382	CIVILINI, MASSIMO	
	Examiner	Art Unit	
	Janet Suglo	2857	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 June 2003* is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 101

1. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claims 1-13 and 22-26 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

A process is statutory if it requires physical acts to be performed outside the computer independent of and following the steps to be performed by a programmed computer, where those acts involve the manipulation of tangible physical objects and result in the object having a different physical attribute or structure (see MPEP 2106). A claim is limited to a practical application when the method, as claimed, produces a *concrete, tangible and useful result*; i.e., the method recites a step or act of producing something that is *concrete, tangible and useful.* Referring to the "Interim Guidelines for Examination of Patent Applications for Patent Subject Matter Eligibility" in determining whether the claim is for a "practical application," the focus is not on whether the steps taken to achieve a particular result are useful, tangible and concrete, but rather that the *final result* achieved by the claimed invention is "useful, tangible and concrete." (<http://www.uspto.gov/web/offices/com/sol/og/2005/week47/patgupa.htm>)

The claimed methods perform processes for electronic component reliability determination. No information is presented to a user nor does a physical transformation occur outside the computer as a result. The claims do not produce a concrete, tangible

and useful result. Therefore the subject matter claimed is considered non-statutory.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. **Claims 1, 4-22 and 24-30** are rejected under 35 U.S.C. 102(b) as being anticipated by Quist et al. (US Patent 6,199,018) (hereinafter "Quist").

With respect to **claim 1**, Quist teaches an electronic component reliability determination method comprising (col 1, ln 4-7):

executing an initialization process (col 20, ln 41-45);

implementing a field condition determination process (collecting temperature data) (Figure 9-2: 101; col 22, ln 40-41);

performing a field condition reliability analysis process (Weibull law) (col 19, ln 46-67); and

performing a reliability information management process (storing information) (col 21, ln 36-39).

With respect to **claim 2**, Quist teaches that the electronic component reliability determination method comprises sensing and tracking initial component startup time after shipping (col 13, ln 46-54; col 16, ln 45-60; col 20, ln 30-37).

With respect to **claims 4 and 5**, Quist teaches that said field condition determination process includes sensing a temperature measurement associated with a component (i.e., machine) (col 8, ln 20-36).

With respect to **claim 6**, Quist teaches establishing an interface for presenting reliability information to a user (col 5, ln 10-15).

With respect to **claim 7**, Quist teaches determining a field condition adjustment factor value (i.e., adjusting the parameters) and instantaneous failure rate value (i.e., initially seeded information about failure) (col 4, ln 56-67).

With respect to **claim 8**, Quist teaches said instantaneous failure rate value is used to determine reliability of a component (col 5, ln 4-18; col 19, ln 46-67).

With respect to **claim 9**, Quist teaches determination of reliability index values (i.e., expected time to failure) for components and a system (col 5, ln 7-18; col 22, ln 57-67).

With respect to **claim 10**, Quist teaches saving parameter information and present value of a reliability indicator (col 21, ln 36-39).

With respect to **claim 11**, Quist teaches a reliability condensing process (col 22, ln 9-27).

With respect to **claim 12**, Quist teaches saving a reliability related reference value (col 28, ln 60-62); receiving an updated reliability related value (col 24, ln 65-67); determining a storage relationship value (i.e., array) (col 25, ln 5-17); and saving said storage relationship value (col 25, ln 5-17).

With respect to **claim 13**, Quist teaches determining a present value of a reliability indicator for a system (col 5, ln 1-3).

With respect to **claim 14**, Quist teaches an electronic component reliability determination system comprising:

a sensor for sensing operation parameter information (col 8, ln 20-36);

a bus for communicating information including said operational parameter information (Figure 1, 2B,C-1,8);

a reliability processing component for performing instructions including instructions for ascertaining a field condition adjusted reliability value (col 19, ln 20-28); and

a memory for saving said operational parameter information and said field condition adjusted reliability value (col 19, ln 20-27).

With respect to **claim 15,** Quist teaches said sensor includes a diode inside a component and said diode is utilized to establish a temperature measurement indication (col 11, ln 3-23).

With respect to **claim 16**, Quist teaches an ambient temperature measuring device (col 9, ln 31-39).

With respect to **claim 17**, Quist teaches air intake and air exhaust temperature measuring components (col 8, ln 20-35; col 9, ln 31-44).

With respect to **claim 18**, Quist teaches using a temperature measurement detected by said sensor to calculate the temperature stress and a reliability adjustment factor (col 4, ln 56-67; col 11, ln 3-47).

With respect tot **claim 19**, Quist teaches performing instructions for calculating an instantaneous failure rate (i.e., initially seeded information about failure) (col 4, ln 56-67).

With respect to **claim 20**, Quist teaches determining an adjustment factor value (i.e., adjusting the parameters) (col 4, ln 56-67).

With respect to **claim 21**, Quist teaches a reliability information condensing process format (col 22, ln 9-27).

With respect to **claim 22**, Quist teaches a computer readable medium with instructions embedded therein for causing a processor to implement a reliability determination process including (col 1, ln 4-7):

an initialization module for directing implementation of an initialization process (col 20, ln 41-45);

a reliability determination background module for directing a field condition determination process (Figure 9-2: 101; col 22, ln 40-41) and a field condition reliability analysis process (col 19, ln 46-67); and

a reliability determination runtime module for interfacing with an operating system (col 12, ln 40-41; col 21, ln 36-39).

With respect to **claim 24**, Quist teaches said background module includes instructions for implementing reliability associated firmware activities (col 12, ln 46-60).

With respect to **claim 25**, Quist teaches said background module divides background tasks into multiple background threads that operate separately (col 6, ln 7-20).

With respect to **claim 26**, Quist teaches calculating instantaneous failure rates (col 4, ln 56-67) and cumulative reliability index values (col 5, ln 7-18; col 22, ln 57-67).

With respect to **claim 27**, Quist teaches a communication device comprising (col 4, ln 18-21):

means for controlling information communication (col 4, ln 6-8);

means for determining component reliability adjusted in accordance with field condition impacts (col 4, ln 56-67); and

means for organizing information associated with said component reliability (col 19, ln 46-67).

With respect to **claims 28 and 29**, Quist teaches means for ascertaining field condition information (i.e., temperature) (col 8, ln 20-36).

With respect to **claim 30**, Quist teaches means for determining component reliability adjusted in accordance with field condition impacts (col 4, ln 56-67) determines an instantaneous failure rate (col 4, ln 56-67) and a cumulative reliability indication (col 5, ln 7-18; col 22, ln 57-67).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. **Claims 3 and 23** are rejected under 35 U.S.C. 103(a) as being unpatentable over Quist et al. (US Patent 6,199,018) in view of Chess et al. (US Patent 5,802,592) (hereinafter "Chess"). Quist teaches initializing random access memory (RAM) with previously stored values (Quist: col 4, ln 56-67; col 16, ln 45-50); defining a reliability sampling period or interval (Quist: col 24, ln 60-64); and starting background tasks (Quist: col 4, ln 56-67). Quist does not explicitly teach checking the integrity of a non volatile memory. Chess teaches verifying the integrity of the contents of ROMs (FLASH and otherwise) (Chess: col 1, ln 37-39). It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the teachings of Quist to include checking the integrity of the non volatile memory as done by Chess because the verification will ensure that no accidental changes have been made to the contents of the ROM (Chess: col 1, ln 39-41).

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Ishii et al. (US Patent 6,671,647) discloses a method and equipment for assessing the life of members put under high in-service temperature environment for long period.

House et al. (US PGPub 2004/0044499) discloses a method and system for determining motor reliability.

Hu (US Patent 5,715,180) discloses a method to reduce sample size in accelerated reliability verification tests.

Barton et al. (US Patent 6,385,739) discloses a self-test electronic assembly and test system.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Janet Suglo whose telephone number is 571-272-8584. The examiner can normally be reached on weekdays from 8:30am - 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Marc Hoff can be reached on 571-272-2216. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Janet L Suglo
April 20,2006

MARC S. HOFF
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800